Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec– 2017**

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| **Code :** | **14EC3024** | **Duration :** | **3hrs** |
| **Sub. Name :** | **LOW POWER VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | A 64 bit off-chip bus operating at 2.5 V and 500 MHz clock rate is driving a capacitance of 50 pF/ bit. Each bit is estimated to have a toggling probability of 0.50 at each clock cycle. What is the power dissipation in operating the bus? | CO3 | 5 |
| b. | Explain about gate level and architectural level power analysis. | CO1 | 15 |
| (OR) | | | | |
| 2. | a. | The chip size of a CPU is 30mm x 50 mm with clock frequency of 600MHz operating at 3.0 V. The length of the clock routing is estimated to be twice the circumference of the chip. Assume that the clock frequency is routed on a metal layer with width of 1.8µm and the parasitic capacitance of the metal layer is 2.0 Ff/µm2. What is the power dissipation of the clock signal? | CO3 | 5 |
| b. | Discuss the variation of short circuit current of a CMOS inverter for input signal slope and output load capacitance. | CO1 | 15 |
| 3. | a. | Apply network restructuring concepts to the circuit Y= ABC + DE. | CO3 | 8 |
|  | b. | Derive the expressions for the power and delay of an inverter chain using transistor sizing. | CO1 | 12 |
| (OR) | | | | |
| 4. | a. | Show gray code encoding and state machine encoding techniques to reduce power with examples. | CO1 | 12 |
|  | b. | Discuss gate reorganization technique to reduce power in logic circuits | CO1 | 8 |
| 5. | a. | Apply Shannon decomposition theorem in the Precomputation Logic Technique to reduce power with an example. | CO3 | 12 |
|  | b. | Show how to reduce switching activity in the circuits to reduce power. | CO1 | 8 |
| (OR) | | | | |
| 6. | a. | Apply various techniques to clock networks of processor chips to reduce Power. | CO3 | 12 |
|  | b. | Write notes on signal gating technique to reduce power. | CO1 | 8 |
| 7. |  | Discuss different low voltage circuit design techniques to reduce power. | CO3 | 20 |
| (OR) | | | | |
| 8. |  | Explain in detail the power and performance management techniques to reduce power in architecture level and also one technique to reduce power in digital filters. | CO3 | 20 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Explain the Banked SRAM concepts and also the techniques to reduce the voltage swing in SRAM design. | CO2 | 10 |
|  | b. | Explain the methods of reducing power in Writer Driver circuits and Sense Amplifier circuits of SRAMcore. | CO2 | 10 |

ALL THE BEST